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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,663	12/01/2003	Radoslav Danilak	NVID-P001159	5113

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EXAMINER	
LEE, CHUN KUAN	

ART UNIT	PAPER NUMBER
2181	

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08/30/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/725,663	DANILAK ET AL.	
	Examiner	Art Unit	
	Chun-Kuan Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 August 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-12 and 14-21* is/are pending in the application.

4a) Of the above claim(s) *2-5,9-11 and 14-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6,8,12 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

CONTINUED EXAMINATION UNDER 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/23/2010 has been entered.

RESPONSE TO ARGUMENTS

2. Applicant's arguments filed 08/23/2010 have been fully considered but they are not persuasive. Currently, claims 7 and 13 are canceled; claims 2-5, 9-11 and 14-20 are withdrawn; and claims 1, 6, 8, 12 and 21 are pending for examination.

3. In response to applicant's arguments with regard to the independent claims 1, 8 and 21 rejected under 35 U.S.C. 103(a) that the combination of the references does not teach/suggest the claimed feature "... a bypass register ... aggregates disk transaction information from memory mapped data transfer from a host CPU ..." because Chisholm does not teach a "memory mapped information transfer" as Chisholm does not teach an information transfer that involves an address that is mapped to an address of the

memory register; applicant's arguments have fully been considered, but are not found to be persuasive.

Please note that the features upon which applicant relies (i.e., an information transfer that involves an address that is mapped to an address of the memory register) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Additionally, it is not fully clear wherein in applicant's Specification discloses that "memory mapped information transfer" is defined as "an information transfer that involves an address that is mapped to an address of the memory register."

I. ELECTION / RESTRICTIONS

4. The examiner recommend that the applicant to cancel the withdrawn claims 2-5, 9-11 and 14-20, as the claimed features of these withdrawn claims have been filed in the divisional applications 12/005,745 and 12/005,816 respectively.

II. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 6, 8, 12, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Chisholm et al. (US Patent 5,968,143), Winkler et al. (US Pub:. 2004/0024948) and Wilcox (US Patent 6,185,634).

6. As per claims 1, 8 and 21, AAPA teaches a computer system, comprising:

executing disk I/O transactions for the computer system (Specification, p. 2, l. 2 to p. 5, l. 4); and

a plurality of CPBs to extend a number of disk transactions (Specification, p. 2, l. 2 to p. 5, l. 4).

AAPA does not teach a disk controller and a bridge component for implementing efficient disk I/O for a computer system, comprising: a bus interface for interfacing … ; a disk controller for executing … : a disk I/O engine coupled to the bus interface; a bus master controller coupled to the disk I/O engine; a bypass register coupled to the bus master controller … ; an arbiter couple to the bus master controller … ; a chain memory coupled to the disk I/O engine … ; and a device interface coupled to the disk I/O engine … .

Chisholm teaches a disk controller and a bridge component for implementing efficient disk I/O for a computer system, comprising:

a bus interface (Fig. 3, ref. 109, 111) for interfacing with a processor (Fig. 1, ref. 103) and a system memory (Fig. 3, ref. 301) of the computer system (Fig. 1-3 and col. 4, l. 26 to col. 6, l. 21);

a disk controller (Fig. 3, ref. 201, 203, 209, 213, 311) for executing disk transactions (Fig. 1-3 and col. 4, l. 26 to col. 6, l. 21), the disk controller further comprising:

a disk I/O engine (Fig. 3, ref. 209, 213) coupled to the bus interface (Fig. 3, ref. 109, 111) (Fig. 1-3 and col. 4, l. 26 to col. 6, l. 21);

a bypass register (Fig. 3, ref. 203, 311) coupled to the disk I/O engine, wherein the bypass register has more than 8 bits is memory mapped and aggregates (e.g. aggregation via transfer to accumulate) of disk transaction information (e.g. command block with transaction information for data transferring) from memory mapped data transfers (e.g. memory mapped data transfers corresponding to the transferring of the command blocks via memory mapping by command block address to the host memory) from a host CPU (Fig. 3, ref. 103) (by using memory mapped data transfer) (Fig. 3-5 and 4, l. 26 to col. 6, l. 21), wherein the register (Fig. 3, ref. 311) is memory mapped as the register comprises the command block address received from the host CPU for transferring of the command/data blocks (Fig. 3, ref. 301) (e.g. transaction information) (col. 5, ll. 25-34), wherein the command block address is mapped to where the corresponding command/data block is located in the host memory (Fig. 3, ref. 107) (Fig. 1-3 and col. 4, l. 26 to col. 6, l. 21);

a chain memory (e.g. section of the memory 203 storing the command blocks 304 of Fig. 3, wherein the memory section is the chain memory storing the chain of command blocks as the addresses (Fig. 3, ref. 309) pointing to these command blocks are in a chain) coupled to the disk I/O engine (Fig. 3, ref. 209, 213) for buffering a

plurality of command blocks (Fig. 3, ref. 304) to extend a number of disk transactions scheduled for execution by the disk I/O engine (Fig. 1-3 and col. 4, l. 26 to col. 6, l. 21); and

a device interface (Fig. 2, ref. 217) coupled to the disk I/O engine (Fig. 3, ref. 209, 213) for interfacing the disk I/O engine with a disk drive (e.g. SCSI RAID disk drives), wherein the disk I/O engine is configured to cause a start up of the disk drive upon receiving a disk start up command (e.g. command transfer start signal) from the processor, the disk I/O engine further configured to execute a disk transaction by processing the disk transaction information (Fig. 3, ref. 304) from the bypass register (Fig. 3, ref. 203, 311) coupled to the disk I/O engine (Fig. 1-3 and col. 4, l. 26 to col. 6, l. 21), as the command/data blocks are transferred to the memory mapped bypass register for implementing disk transaction and bypass the writing of a set of 8 bit registers in the disk controller as implemented in ATA disk drives.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include Chisholm's interfacing architecture into AAPA's computer system for the benefit of increasing data transferring throughput by reducing the command block transfer overhead (Chisholm, col. 2, ll. 20-50 and col. 5, ll. 55-58) to obtain the invention as specified in claims 1, 8 and 21.

AAPA and Chisholm do not teach the disk controller and the bridge component for implementing efficient disk I/O for the computer system, comprising: a bus master

controller coupled to the disk I/O engine; an arbiter couple to the bus master controller … ; and causing the start up before completion of said start up ….

Winkler teaches a system and a method comprising:

a bus master controller coupled to a disk I/O engine (e.g. hard disk controller) ([0013]), by combining the bus master controller with AAPA and Chisholm's bypass register and disk I/O engine, the resulting combination further teaches the bypass register which is coupled to the disk I/O engine is coupled to the bus master controller; and

an arbiter coupled to the bus master controller and the disk I/O engine (e.g. hard disk controller), to coordinate data transfers within the disk controller ([0013]), wherein the inclusion of the arbitration function into the disk controller would enable proper coordination of the data transferring for disk drive system such as RAID.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include Winkler's bus master controller and arbitration into AAPA and Chisholm's disk controller for the benefit of increasing the operation speed, as well as improving reliability and the efficiency in the transferring of data (Winkler, [0017]) to obtain the invention as specified in claims 1, 8 and 21.

AAPA, Chisholm and Winkler do not teach the disk controller and the bridge component for implementing efficient disk I/O for the computer system, comprising causing the start up before completion of said start up ….

Wilcox teaches a system and a method comprising: causing the start up before completion of said start up, the start up command configured to hide a start latency of the disk drive (Fig. 7; col. 2, ll. 10-23; col. 3, ll. 40-62; col. 5, ll. 7-41; and col. 11, l. 38 to col. 12, l. 57), as the delay to for the start up of data transferring is hidden.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include Wilcox's start up into AAPA, Chisholm and Winkler's disk controller for the benefit of reducing latency in the transferring of data to the disk drive (Wilcox, col. 1, ll. 19-23 and col. 2, ll. 51-53) to obtain the invention as specified in claims 1, 8 and 21.

7. As per claims 6 and 12, AAPA, Chisholm, Winkler and Wilcox teach all the limitations of claims 1 and 8 as discussed above, where AAPA, Chisholm and Winkler further teach the disk controller further comprising: a CPB pointer buffer (Chisholm, command address queue 309 of Fig. 3) coupled to the disk I/O engine for dynamically appending a plurality of CPB pointers (e.g. addresses pointing to where the command block are stored) to extend to a number of disk transactions scheduled for execution by the disk I/O engine, the CPB pointer buffers (Chisholm, Fig. 3, ref. 309) directly connected to the disk I/O engine (Chisholm, Fig. 3, ref. 209, 213) for control independent of the arbiter (AAPA, Specification, p. 2, l. 2 to p. 5, l. 4; Chisholm, Fig. 1-3; col. 4, l. 26 to col. 6, l. 21; and Winkler, [0013]).

III. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1, 6, 8, 12 and 21 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chun-Kuan Lee/
Primary Examiner
Art Unit 2181
August 30, 2010